CPU-free Computing: A Vision with a Blueprint

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ABSTRACT

Since the inception of computing, we have been reliant on CPU-powered architectures. However, today this reliance is challenged by manufacturing limitations (CMOS scaling), performance expectations (stalled clocks, Turing tax), and security concerns (microarchitectural attacks). To re-imagine our computing architecture, in this work, we take a more radical, but pragmatic approach and propose to eliminate the CPU with its design baggage from data center computing. We integrate three primary pillars of computing, i.e., networking, storage, and computing, into a single, self-hosting, unified *CPU-free* Data Processing Unit (DPU) called Hyperion. The elimination of the CPU from computing necessitates re-thinking our computing, networking, and storage abstractions, and tackle the associated challenges which we sketch in this paper. We share the blueprint of our work-in-progress, Hyperion's hardware and software stack, and seek feedback.

CCS CONCEPTS

• **Hardware** → **Hardware accelerators**; **Reconfigurable logic and FPGAs**; *Hardware description languages and compilation*; • **Software and its engineering** → *General programming languages*; **Operating systems**; **Secondary storage**; **Secondary storage**.

KEYWORDS

CPU-free computing, Accelerators, Programming, Data storage, Data Processing

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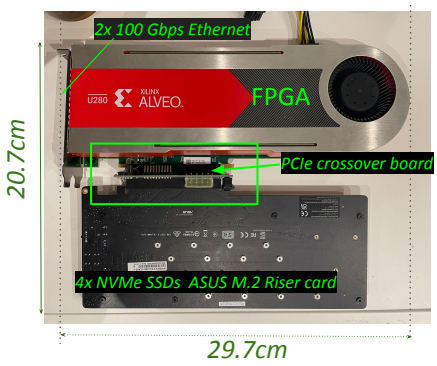

Figure 1: A CPU-free Hyperion prototype with a unified 100 Gbps network, U280 FPGA, and NVMe SSDs.

1 INTRODUCTION

Since the inception of computing, we have been designing and building computing systems around the CPU as the primary workhorse. This primary architecture has served us well. However, as the gains from Moore's and Dennard's scaling for the CPU start to diminish (Turing tax, complexity, security challenges [36, 56, 57, 70, 97]), researchers have started to look beyond the CPU-centric design to domain-specific accelerators such as GPUs [27, 86, 140], TPUs [83], computational storage devices (CSDs, NVMe TP-4091) [105, 141, 146], SmartNICs [55, 157], Reconfigurable Architectures (CGRAs [166] and FPGAs [100, 135]). The use of *specialized* domain-specific hardware in mainstream computing is heralded as the *Golden Age of Computer Architecture* by Hennessy and Patterson in their Turing Award lecture [71].

The CPU Problem: However, even in this Golden Age, the CPU[1] remains in the critical path to manage data flows [137] (data copying, I/O buffers management [122]), accelerators (e.g. complex PCIe enumerations [145]), and translate between OS-level (packets, processes, files) to device-level abstractions (memory and block addresses) [17, 73, 153, 158]). Much of the current state-of-the-art efforts are still focused on minimizing the CPU involvement in control and data paths between the accelerators (see Table 1). Additionally, accelerator integration is always done (via virtualization or multiplexing) while keeping the CPU and accelerator view of systems resources (DRAM, memory mappings, TLBs) coherent and secure. Though necessary, such an integration brings

[1] referring to the CPU from the host (e.g. x86) as well as smart accelerators like ARM-based SoC and SmartNICs.

GPU-with-network [93, 125]	Does not have or consider any storage integration
GPU-with-storage [23, 26, 124, 137, 151]	CPU-assisted storage translation, no or limited networking support
FPGA/ARM SoC-with-Network [37, 54, 58, 113, 134, 135]	Does not have or consider storage integration
Storage-with-Network [75, 95, 109, 126, 142]	Block-level protocols only (iSCSI, NVMoF), no support for file systems
Storage-with-accelerator [27, 67, 80, 87, 99, 141, 144, 146]	CPU does the file system/translations, no/limited network support
Commercial domain-specialized DPUs [59, 126, 131]	DPU designed around specialized CPU cores (P4, ARM, MIPS64)

Table 1: Overview of the state-of-the-art efforts in decreasing the CPU involvement in computing *while* maintaining CPU-centric memory and storage abstractions when doing *pair-wise* accelerator interactions.

complexity in the accelerator management and keeps the CPU as the final resource arbiter. We are not the first ones to raise issues associated with the CPU-centric computing or the CPU overheads with accelerators [16, 47, 123, 150] (see Related work in §3). However, unlike the previous efforts, we are making a case that it is not only the CPU, but the CPU-associated, CPU-centric abstractions (processes, virtual memory, coherency, sharing, caches, storage-memory hierarchy) that need to be reconsidered as well. The design of these abstractions predate the emergence of accelerators. Without re-imagining, the CPU and consequently, the CPU-centric computing abstractions remain in the critical path of end-to-end system building, thus not escaping the dynamics of Amdahl's Law.

A case for CPU-free computing: In this work, we enquire a more foundational and far-reaching question: *how would computing look today if we were only given accelerators to design a computing system from scratch?* Our position for CPU-free computing is inspired from the challenges around:

(1) *Shared and coherent virtual memory:* A direct consequence of keeping a CPU-centric design is to inherit its choices of memory addressing, translation, and protection mechanisms. When an accelerator such as an FPGA[2] is attached to a CPU as an external device [41] or as a co-processor [44], there is a temptation to provide/port the familiar memory abstractions like unified virtual memory [100] and/or shared memory [115]. Virtual memory is a deceptively simple idea [50] whose implementation on modern CPUs with multicore, caches, nested page tables, prefetchers, virtualization, TLBs, IOMMUs have been known to be a source of major complexity, overheads, security vulnerabilities, and energy inefficiencies [22, 45, 65, 154]. When an accelerator (GPUs, FPGAs, CSDs) is integrated with a CPU-centric host system, it multiplies this complexity in an attempt to keep the CPU's view of the system coherent [100, 115]. ETH's Enzian system, which is a hybrid CPU-FPGA dual socket system, reports the heroic engineering effort it took to re-design all systems components to integrate an FPGA as a co-processor *with a CPU* [44]. Not only the virtual memory, but the CPU's view a flat, physical memory is also outdated in presence of multiple accelerators [9].

(2) *Persistence and storage hierarchy:* Due to the two-level of storage/memory hierarchy, both DRAM (memory) and storage use different storage abstractions. Examples of storage abstractions are block-oriented formats (e.g., file formats ORC, Parquet [159]), files, directories, data structures (B+/LSM trees), etc. DRAM uses ephemeral pointer-based data structures in virtual memory. As a result, there is an abstraction translation process done by the CPU (and systems software) whenever storage is accessed by an accelerator to translate storage abstraction (*data-at-rest*) to memory abstraction (*data-in-motion*). Recent works in persistent memory heaps, file systems, and OS designs grapple with the translation complexity, and question even if there is a need for such a translation [31, 43, 74, 85, 110]. No significant improvements are expected in the process of abstraction translations as very modest CPU performance improvements are projected in the future [1, 78].

(3) *Disaggregation:* The CPU-centric design encourages the *active* resources disaggregation where resources remain attached to a host CPU that manages the disaggregation logic. This design results in a coarser disaggregation granularity with complex and bloated software [60] and a tight integration of processor/memory [68, 147]. To achieve the vision painted by Han et al. in their seminal HotNet'13 paper [69], there is a renewed push for *passive* disaggregation where the disaggregation logic/smartness lies with clients, and a remote resource only serves fast datapath requests [13, 38, 68, 147, 160]. Passive disaggregation promotes a *network-attached model*, where self-hosting memory, storage, DPUs, and ASICs are directly connected to a network. Such a design encourages innovations in: (i) discovery and configuration network protocols (e.g., Catapult fabric [135]); (ii) work division between clients and remote servers for distributed resource allocation, and access (e.g., Clio [68], DUA [149]); and (iii) offload-friendly abstractions with isolation, multiplexing mechanisms (e.g., group offloading and memory re-assignments [13, 92, 112]).

[2]Using an FPGA as a canonical example for broader non-CPU devices.

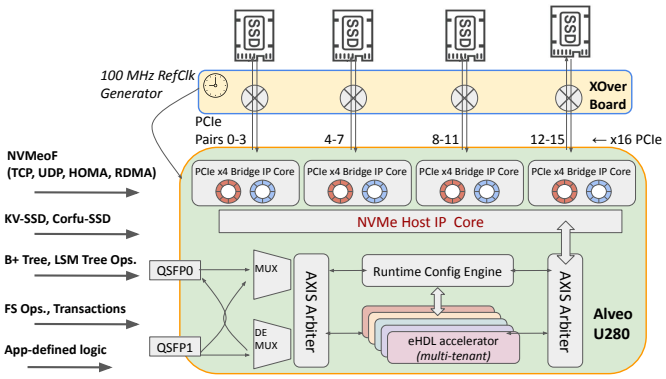

Figure 2: Schematic diagram of the Hyperion.

To summarize: The first-principle reasoning suggests a solution to tackle the aforementioned challenges: a system where there is no CPU, i.e., a CPU-free architecture. The CPU-centric design has its merits (with challenges), and its elimination is *not recommended* for every workload in general computing. Here we focus on specialized, accelerator-amenable data center workloads for which we aim to explore the CPU-free design space (see §2.4).

2 DESIGNING A CPU-FREE SYSTEM

In order to explore the CPU-free computing design space, in this work, we design a CPU-free DPU called Hyperion. The DPU is built around a Xilinx Alveo U280 board with 2x100 Gbps Ethernet QSFP [2], a PCIe cross overboard [51] to attach 4x NVMe devices to the U280 with power (figure 1). Commercially, NICs and storage devices are sold as separate PCIe devices. Communication between the two requires control coordination with P2P DMA from the CPU (if supported, e.g., NVMe Controller Memory Buffers (CMBs) [24]) via the PCIe root complex. To make the DPU self-hosting, Hyperion runs a PCIe root complex with an NVMe controller on the FPGA board. The FPGA (x16) PCIe lanes are connected to off-the-shelf NVMe storage devices via a PCIe bifurcation. Hence, all access to the storage is funneled through the FPGA. Hyperion follows the directly network-attached model that has been used before [80, 135, 149, 164], but extends it with storage integration. With such a design, Hyperion now has an *end-to-end hardware path* from network to FPGA to storage devices without any CPU. The end-to-end hardware path can be *specialized* with workload-specific abstractions with an application-defined network transport (TCP, UDP, RDMA, HOMA [127]), storage API (NVMoF [142], KV [28], ZNS [32]), and optimizations [75, 76, 95, 121].

The DPU boots in a *stand-alone mode* without any CPU when power is applied and FPGA JTAG self-tests are passed. The DPU is currently attached to a host-system via USB for programming. We are in the process of developing an OS-shell and control path over the network that can program the FPGA without a CPU, leveraging Partial Dynamic Reconfiguration through the Internal Configuration Access Port (ICAP) of the FPGA. In comparison to a conventional 1U rack-mounted server like SuperMicro X12, Hyperion is 5-10× more compact in volume, and 4-8× more energy efficient with the maximum TDP energy specifications (approx. 230 Watts vs 1,600 Watts). Figure 2 shows the overall schematic diagram of the different components and how they are connected on the hardware level.

In comparison to past such efforts, Hyperion presents a complete, self-hosted, network-attached system that does not rely on any host CPU/OS services to support workloads, thus reducing the integration complexity and overheads. Hyperion can be used as a (low-cost) research platform to explore various CPU-free hardware and software techniques.

The choice of FPGA to explore the CPU-free model is governed by its three strengths: (1) *Application-specific reconfigurability:* The use of FPGA allows us to reconfigure hardware (deep pipelines, unrolled loops, data parallelism, large caches, memories: SRAM, DRAM, or HBM) to the best possible implementation for a wide variety of application-specific logics [8, 12, 40, 96, 161]. (2) *Improved FPGA systems software support:* With the availability of high-quality DSLs [19, 79, 98, 143], OS-shells [89, 100], HDL DSL compilers [37], and debuggers [116, 167], it has become more affordable to generate high-quality HDL codes. (3) *Predictable performance with energy efficiency:* FPGAs excel in coarse-grained spatial multiplexing with longer time-scales (10-100 msecs, partial reconfiguration) [89, 100]. This sharing model helps with building a highly *predictable execution pipeline* where once an associated bitstream has been sent to the FPGA, the circuit runs a certain clock frequency without any outside interference, thus delivering energy efficient [37, 136, 141] and predictable performance [81, 108]. As the availability of open-source EDA processes and projects improve, in the future we can explore workload-specific ASIC-centric IP designs as well [3, 5].

2.1 Memory and Storage Model

Not having any host-attached CPU resources makes the integration of the memory and storage model less complex. In Hyperion, we leverage a segmentation-based, single-level unified storage-memory addressing with 128-bits objects (inspired from Twizzler [31]). In the current implementation, we statically divide FPGA AXI-streaming bus address ranges to map to FPGA DRAM addresses, and others to NVMe PCIe BAR addresses. Hence, the total addressable capacity is DRAM plus NVMe storage capacities. The segment location translation is done using a segment translation table that maps a segment id (128 bits) to their bus addresses and

to their location, DRAM or NVMe. The current allocation of segments to their locations (DRAM or NVMe) is static. It is done based on their bus addresses. However, we expect hints-based allocation should also be possible where temporary and/or performance-critical objects are allocated or eventually promoted to DRAM or HBM. One can treat all segments as ephemeral and use NVMe just as a large capacity location. When durability is required, all durable segments must also be allocated on NVMe addresses. The segment translation table is periodically persisted on a pre-selected control/boot NVMe area. The unique aspect of segmentation-based location translation is that it is coarser (object-based) than virtual memory (page-based), thus reducing overheads associated with the virtual memory translation [10].

Segmentation-based addressing is already in use with FPGAs with heterogeneous memory locations [11, 89]. Single-level data stores like MULTICS and Atlas [46, 91] pioneered the idea of hiding an object's location and are precursor to the virtual memory idea. Due to the ephemeral nature of memories, the addressing mechanism with memories were never integrated with the storage to make them durable. IBM AS/400 [77] and EROS [148] are closest to our approach with single-level, segmentation-based persistent objects. In the future, as more accelerator are integrated in Hyperion, we consider leveraging the CXL protocol to support application-specific coherence, if required [64, 84].

2.2 Programming the Hyperion DPU

Inspired by the LLVM project, in this work, we argue that FPGA programming needs to decouple the frontend (application logic) and backend (HDL codes) with an accelerator-independent, intermediate representation (IR) language. The IR can be used to reason about correctness and safety properties of the program, with compiler-assisted transformations for pointer swizzling and privilege calls. We make a case that the extended Berkeley Packet Filter (eBPF) [42, 120] language is a suitable match for such an IR for three key reasons. First, eBPF is not tied to a specific application-domain and it is used in networking [7, 72], tracing [66], caching [62], security [88], and (very successfully) storage [21, 29, 101, 114, 173]. It is also supported by healthy, growing communities (Cilium, the eBPF foundation), thus establishing expertise and a knowledge base. Second, due to the simplified nature of the eBPF instruction set, it is possible to verify and reason about its execution. The Linux kernel already ships with an eBPF verifier [156] (with simplified symbolic execution checks). Lastly, eBPF supports efficiently generating codes for multiple hardware devices such as x86, ARM, or FPGAs, thus solidifying its position as an accelerator-independent unifying IR [90].

Bear in mind, here we take a broader position regarding eBPF where the Linux kernel implementation is one of many possible implementations of an eBPF execution environment. For example, there are userspace BPF VMs [6], checkers [61], and application-specific ISA extensions [37]. Hyperion can use any eBPF-supporting programming language as a frontend. It then uses `clang/LLVM` to generate eBPF IR from the frontend. We are developing a code generation pipeline from eBPF-to-HDL using a set of open-source compilers for parallelism extraction, and then eBPF instructions specific HDL code generation, fusion, and wrapping in hardware [35, 37, 139]. Apart from eBPF, we also consider P4, another popular programming language for in-network acceleration (NICs and switches). However, P4 programs are designed around packet processing and network abstractions. In restricted capabilities (with only filtering and forwarding), there are P4 to eBPF compilers available, though the generality of P4 for general data processing is yet to be explored.

We expect to leverage the already established slot-style spatial slicing of FPGA resources [89, 100] or a compiler-assisted workload partitioning for multi-FPGA deployments [170]. Hyperion can run a privileged configuration kernel that can receive authorized, encrypted FPGA bitstreams over a certain control network port and assign slices to it.

2.3 Storage Abstractions: Files and Objects

Beyond supporting block-level offloaded accesses to storage (NVMoF), in this section we explore how Hyperion can support higher-level familiar abstractions like file systems and workloads-level data objects without any CPU support. The key challenge here is how to resolve a higher-level object such as a columnar data to its storage location where multiple storage layers (formats, file systems) do abstraction translation. Inspired by the Internet that decouples packet processing from its well-defined packet formats (e.g., the TCP/IP formats), we propose to decouple data formats from their accessing explicitly using an annotation-based, domain-specific language (DSL). Starting at the file-system level, prior research from Sun et al. show that such a file-system layout annotation can be generated efficiently for ext4 and F2FS files systems [155]. The availability of annotation enables us to generate file system layout and metadata access codes (in C/C++), thus accessing directories and files directly. These annotated codes can further be translated to HDL codes using the Hyperion compiler. As a next step, we target well-defined application-level object formats Parquet (on storage) and Arrow (in-memory) that are used in a variety of data processing pipelines [14, 15] with FPGA support for their formats [103, 130]. With the file system access annotation, we expect to build an end-to-end Parquet/Arrow object access pipeline in hardware with end-to-end optimizations [129]. With such capabilities, Hyperion can access and process data that is stored in Arrow/Parquet format, on the F2FS/ext4 file

system on NVMe storage without any host-side, or client-side CPU involvement. A file-, object-, or datastructure-based interface to storage can co-exist in Hyperion.

2.4 Client Interface and Workloads

There are two classes of workloads here: (C1) mixed distributed workloads where a mix of CPU servers and CPU-free Hyperion DPUs run in a distributed networked; and (C2) pure Hyperion workloads where an application runs completely in a CPU-free mode over one or multiple DPUs. Currently we are focusing on developing the latter (C2) for a single DPU with three applications. First, high data volume network middleware applications such as fail2Ban [4] or load-balancers [169]. These applications have traffic-flow proportional states that either need to be persisted (in case of fail2Ban that needs to log network traffic data persistently) or require large temporary data storage (e.g., Tiara offloads load-balancing state from FPGAs to x86 servers [169]). These network middleware applications can run in a pure, stand-alone mode on Hyperion with attached SSDs. Second, a latency-sensitive application such as network pointer-chasing. In a disaggregated storage, pointer chasing over B+ trees, extent trees, LSM trees (used in many databases, file systems, and key-value stores [133]) results in multiple network RTTs with significant performance degradation [101, 104]. These latency-sensitive applications can now be deployed in the FPGA even if they access higher-level data objects. Lastly, network-attached SSDs that can export application-defined, high-level, fault-tolerant data structures and abstractions (pioneered by Boxwood [117]) such as trees, lookup-tables [28], distributed/shared ordered logs [20, 165], atomic writes [128] with transactional interfaces (left side of figure 2).

For mixed, distributed workloads, we take inspiration from the flexible RPC interface pioneered by Willow [146]. The RPC interface can be *specialized* end-to-end with network, storage, and application-level protocols. For example, we can build network-attached SSDs that can support Corfu consensus protocol [20, 165], or remote file system access acceleration with DPUs using `virtio-fs` [63, 132], or RDMA acceleration for a flash file system [158], or the bump-in-the-wire/near-data execution of application-provided codes (B+/LSM tree search, compaction and insertions, file system walks, transactions) [141, 171]. Here, we can leverage client-driven request routing [111] with a shared-nothing, run-to-completion data path [25] for performance. Further possibilities exist with network transport and scheduling optimizations [75, 76, 121, 127]. As more applications get developed, there will be a need to manage end-to-end CPU-free design patterns efficiently, with possibilities of sharing and composibility among different workloads even in presence of failures [162].

2.5 Compilers as the new operating system?

Due to the absence of the conventional CPU, doing the classical resource arbitration with elevated privileges to mediate accesses to a shared resource in Hyperion would be challenging. There is no clear abstraction of different protection-levels as envisioned by the classical UNIX-style OS designs. Hence, we must re-negotiate the work division among the hardware, a compiler, and an application with the compiler taking a leading role to deliver translation, multiplexing, and isolation properties — the traditional roles of an OS. With this compiler-centric approach, we run the risk of repeating the failure of the VLIW processors[3]. We argue that there are two fundamental shifts that work in our favor. First, domain/workload-specific architectures are common, and associated languages and compilers are used extensively as the norm. There are significant research and commercial interests in co-designing domain- or workload-specific hardware/software. Second, unlike VLIW processors, a DPU (specifically FPGA driven) is not aimed at delivering performance for *all or any* workloads, hence restricting the optimization design space. The role of compiler is not unusual here. It supports many OS-level roles already for services like Unikernels with specialization via compilation, end-to-end optimizations of various components [129], and a reduction of attack surfaces by dynamic recompilation [102]. Even with hardware/FPGAs it has been shown that the compilers can assist with traditional OS roles such as context switching [52, 106, 118], memory virtualization [154], single-level memory/storage [31, 74], isolation [107], extraction of parallelism [37], virtualization and multi-tenancy [89, 170].

3 RELATED WORK

Nider and Fedorova also question the utility of "the Last CPU" in the system and investigate the design of a *system management bus* (hardware) with autonomous devices to take over the OS/CPU responsibilities [123]. However, they still rely on shared, virtual memory (with IOMMU) as the core abstraction around which smart devices are integrated, and data identification, access, and processing happens. The CPU is removed from its managerial role, while the CPU-centric abstraction of a shared, coherent virtual memory is kept, hence inheriting and perpetuating the complexity with (virtual) memory management with accelerators [9, 22, 45, 65, 109, 154]. Furthermore, in comparison to their proposal which requires changes to the current architecture in hardware (a new management bus, and new types of devices), Hyperion is more pragmatic that can be

[3]VLIW compilers were left responsible for parallelism extraction in general workloads, which lead Donald Knuth to comment that *"…the "Itanium" approach that was supposed to be so terrific—until it turned out that the wished-for compilers were basically impossible to write"* [30].

realized today with the help of compilers. Omni-X system proposes to "exterminate the CPU" for inter-accelerator communication, and use P2P DMA for control/data coordination while still relying on CPU-centric abstractions in a multi-kernel/unikernel setting (coherent, shared virtual memory, file descriptors, sockets) [150]. M^{3}X system does not need shared coherent memory for inter-device communication and with the OS services, but requires explicit hardware support for network-on-chip communication endpoints between accelerators [16]. The MSR BEE3 system (used for emulation) is an early example of a complete non-CPU-centric system design [49].

Table 1 shows past research for *pair-wise device* interactions efforts where the role of the CPU is minimized or eliminated such as GPU-with-storage [23, 26, 27, 137, 151], GPU-with-network [48, 93, 125], accelerator-to/from-storage [16, 18, 109], SmartNICs [55, 134, 157], and networked storage accesses [94, 142]. FPGAs are explored with (1) networks [37, 58, 163, 174]; and (2) storage [141, 144, 146]. (e)BPF offloading to NIC/FPGA for processing is done with Endance DAG cards [53], Netronome [82], Combo6 [119], but mostly limited to monitoring and traffic shaping. FPGA-assisted KV stores have considered a close integration of network and KV processing (in-memory) [33, 39, 80, 108] and selective integration of NAND flash (e.g., BlueDB and Xilinx-KV [34, 168]). Project Alkali combines FPGA SoC with Cortex CPUs to design a computational storage device (CSD) designed to accelerate TensorFlow ML workloads from NVMe storage [87]. It uses eBPF (on the CPU with uBPF) with TensorFlow Lite with a possibility of ML operator specialization in FPGA with Chisel and TVM/VTA frameworks. However, even with that it is the CPU that drives the NVMe FPGA data orchestration logic for workflow execution. In comparison to these efforts, Hyperion targets a broader design space, where we explore new types of system design with a unified reconfigurable hardware (FPGA), network transport (100 Gbps Ethernet), and storage (NVMe flash). This unification offers end-to-end exploration of novel full-system CPU-free abstractions and with specializations to support emerging workloads like serverless and disaggregation.

4 DISCUSSION AND FEEDBACK

Hyperion is still in its early prototyping phase. From the systems community, we seek feedback on issues like:

(1) Is eliminating the CPU a worthy pursuit? In this paper, we made an ambitious case for removing the CPU. We believe that with the recent hardware/software advancements it is the right time to re-evaluate the role of the CPU and its design baggage. However, we are interested in hearing counter-arguments. We realize that engineering, development, and prototyping complexities might put limits to the realization of this idea. At what levels of performance, energy, and packaging efficiency gains from a CPU-free design will make the idea worth while? The elimination of the CPU-side mediation also necessitates a bigger supporting role from the FPGA toolchains, languages, and compilers, a role which was previously split between the host CPU and OS. Are FPGA toolchains ready?

(2) What are the killer workloads? Currently, our focus is on developing a familar set of reusable core storage abstractions such as trees (B+, LSM), hash tables, and graphs that can leverage the heterogeneous computing, memory, and storage resources available in Hyperion. Using these core data structures, we can build various key-value stores, network services (load balancers, packet loggers), and end-to-end workload-specialized DPUs, e.g., analytics (TPC, OLTP), LDBC Graphalytics with graph database, Bioinformatics (genome assembly), or climate modeling — all workloads which are data-intensive and have been shown to benefit from FPGA acceleration [152, 161]. Here we seek feedback on identifying specific high-priority workloads that can help us explore the abstraction design space.

(3) What is the right client-interface to build *distributed* Hyperion applications? Looking beyond a single DPU, what kind of application-level abstractions are required for building *distributed* CPU-free applications that can be executed over multiple DPUs? How should one build CPU-free distributed applications and composable service ecosystems of such standalone, passively disaggregated DPUs? Can such CPU-free ecosystems exist, or is a mixed CPU and CPU-free Hyperion setup a more realistic model?

(4) Complexity in multi-tenant clouds? In data centers, hardware and software fail. Tenants are untrusted. The costs of inefficiency and downtime are high. Hence, how to ensure that Hyperion can offer a secure, multi-tenant execution over multiple FPGAs [172]? How to reduce microarchitectural attacks with Hyperion? Can or should the micro-architectural resources of Hyperion be managed explicitly with tenants to ensure sufficient isolation with Hyperion DPUs [138]?

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